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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,602	10/01/2003	Jau-Wen Chen	03-0717	7921

24319 7590 03/24/2005

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,602	CHEN ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-19* is/are rejected.

7)☒ Claim(s) *12 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/1/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 12 is objected to because of the following informalities: in line 2, "pMOSFE.T" is a typographical error and should be spelled "pMOSFET." Appropriate correction is required.

Claim 15 is objected to because of the following informalities: in line 3, "filte" should be spelled "filter." Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12, 15, and 20 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 12 and 20 recites the limitation "the diffusion ring" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim. The claim is rendered indefinite because it is not understood structurally how the source of the pMOSFET is connected to the device.

Claim 15 recites the limitation "the well ring" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim. The claim is rendered

indefinite because it is not understood structurally how the VDD is connected to the device.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Hirata et al. (US 6,469,354 B1).

In re claim 1, Hirata et al. shows (fig. 8B) a semiconductor device comprising: a semiconductor substrate (10) a first well region (11a) formed on a surface region of said semiconductor substrate, said first well region having therein at least one MOS transistor and having at least one NMOS finger (15n) thereon; a second well region (11b) formed on a surface region of said semiconductor substrate; and a well ring (27) formed on a surface region of said semiconductor substrate and disposed between said first well region and said second well region, said well ring configured such that said first well region is separated from said second well region other than through a resistance of the semiconductor substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al. (US 6,469,354 B1) as applied to claim 1 above, and further in view of Ker et al. (US 6,750,517 B1).

In re claims 2 and 3, Hirata shows all of the elements of the claims except the resister disposed between the gate and VSS. Ker et al. discloses (col. 1, lines 45-54) that a resistor is disposed between a gate of the NMOS and VSS to prevent gate oxide breakdown of the gate during an ESD overstress condition. Ker does not specifically disclose that the gate is configured as a high pass filter but the resistor and gate are inherently configured to act as a high pass filter because the structure and materials are the same as the applicant's claimed invention. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the NMOS fingers of Hirata by adding a resistor between the gate and VSS as taught by Ker to prevent gate oxide breakdown of the gate during an ESD overstress condition.

Claims 4 and 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al. (US 6,469,354 B1) as applied to claim 1 above, and further in view of Chen et al. (US 6,750,517 B1).

In re claim 4, Hirata shows all of the elements of the claims except the well ring connected to VDD. Chen et al. shows (fig. 4) an ESD device comprising a well ring (146) connected to VDD to prevent latchup of the NMOS device (col. 4, lines30-62). Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the well ring of Hirata by supplying it with a voltage VDD as taught by Chen to prevent latchup of the NMOS device.

In re claims 6-11, Chen shows (fig. 4) that a diffusion ring (148) is disposed between the well ring (146) and the NMOS region. The diffusion ring is connected to a pMOSFET (110 via contact 116) and inherently functions as a trigger node because it has the same materials and structure as the applicant's claimed invention. Figure 3 shows that the well ring surrounds the diffusion ring. The diffusion ring (148) is connected to VSS.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al. (US 6,469,354 B1) as applied to claim 1 above, and further in view of Ker et al. (US 6,750,517 B1) and Chen et al. (US 6,750,517 B1).

In re claim 5, Hirata all of the elements of the claims except the resister disposed between the gate and VSS. Ker et al. discloses (col. 1, lines 45-54) that a resistor is disposed between a gate of the NMOS and VSS to prevent gate oxide breakdown of the gate during an ESD overstress condition. Ker does not specifically disclose that the gate is configured as a high pass filter but the resistor and gate are inherently configured to act as a high pass filter because the structure and materials are the same

as the applicant's claimed invention. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the NMOS fingers of Hirata by adding a resistor between the gate and VSS as taught by Ker to prevent gate oxide breakdown of the gate during an ESD overstress condition.

Hirata and Ker show all of the elements of the claims except the well ring connected to VDD. Chen et al. shows (fig. 4) an ESD device comprising a well ring (146) connected to VDD to prevent latchup of the NMOS device (col. 4, lines30-62). Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the well ring of Wu by supplying it with a voltage VDD as taught by Ker to prevent latchup of the NMOS device.

There is no prior art rejection for claim 12.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al. (US 6,469,354 B1) in view of Ker et al. (US 6,750,517 B1).

In re claims 13 and 14, Hirata et al. shows (fig. 8B) a semiconductor device comprising: a semiconductor substrate (10) a first well region (11a) formed on a surface region of said semiconductor substrate, said first well region having therein at least one MOS transistor and having at least one NMOS finger (15n) thereon; and a second well region (11b) formed on a surface region of said semiconductor substrate. Hirata shows all of the elements of the claims except the resister disposed between the gate and VSS. Ker et al. discloses (col. 1, lines 45-54) that a resistor is disposed between a gate

of the NMOS and VSS to prevent gate oxide breakdown of the gate during an ESD overstress condition. Ker does not specifically disclose that the gate is configured as a high pass filter but the resistor and gate are inherently configured to act as a high pass filter because the structure and materials are the same as the applicant's claimed invention. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the NMOS fingers of Hirata by adding a resistor between the gate and VSS as taught by Ker to prevent gate oxide breakdown of the gate during an ESD overstress condition.

Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata et al. (US 6,469,354 B1) in view of Ker et al. (US 6,750,517 B1) as applied to claim 13 above, and further in view of Chen et al. (US 6,750,517 B1).

In re claim 15, Hirata and Ker shows all of the elements of the claims except the well ring connected to VDD. Chen et al. shows (fig. 4) an ESD device comprising a well ring (146) connected to VDD to prevent latchup of the NMOS device (col. 4, lines30-62). Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the well ring of Hirata and Ker by supplying it with a voltage VDD as taught by Chen to prevent latchup of the NMOS device.

In re claim 16-19, Chen et al. shows (fig. 4) that a diffusion ring (148) is disposed between a well ring (146) and the NMOS region. The diffusion ring is connected to a pMOSFET (110 via contact 116) and inherently functions as a trigger node because it has the same materials and structure as the applicant's claimed invention. Figure 3

shows that the well ring surrounds the diffusion ring. The diffusion ring (148) is connected to VSS.

There is no prior art rejection for claim 20.

Allowable Subject Matter

Although claims 12 and 20 were rejection above under 35 USC 112, the claims contain allowable subject matter. If the 112 Rejection is overcome, the claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Salling et al. (US 6,858,902 B1) is particular relevant to the invention but does not qualify as prior because of its filing date. Wu (US RE 38,222E) and Lee et al. (US 6,329,694 B1) also disclose ESD protection devices having resistors connected to gates and well rings between substrate wells.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
March 20, 2005

GEORGE ECKERT
PRIMARY EXAMINER